THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte STEPHAN GUNTHER,
And CHRISTOPH KUNDE

_____

Appeal No. 97-0280
Application 08/192,839[1]

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ON BRIEF

_____

Before KRASS, FLEMING and TORCZON, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 4 and 6 through 21, all of the claims pending in the present application. Claim 5 has been canceled. On page 4 of the Examiner's answer, the Examiner has withdrawn the

[1] Application for patent filed February 7, 1994.

rejection of claims 2, 4 and 6 through 15 and has allowed these claims. Therefore, claims 1, 3 and 16 through 21 remain rejected and are properly before us for our consideration.

The invention relates to a method for storing security relevant data in a postage meter, in which the same data is stored in several memory areas.

The independent claim 1 is reproduced as follows:

1. A method for storing security relevant data in a postage meter, in which method data (A, B, C, D) are stored in several memory areas (a, b, c, d), the data (A, B, C, D) are read out of the memory areas (a, b, c, d) and the data of one memory area is compared with the data of another memory area, and in which a memory area with faulty data is ascertained, if such memory area with faulty data exists, said method comprising the steps of:

storing the same data (A, B, C, D) in at least four memory areas (a, b, c, d),

making comparisons to compare the data (A, B, C, D) of each memory area (a, b, c, d) with the data (A, B, C, D) of the other memory areas (a, b, c, d) and to produce results indicating for each comparison whether the data compared is in agreement or not in agreement,

ascertaining a fault number (Z) which fault number (Z) indicates in how many of said comparisons lack of agreement is found between the compared data, and

processing the results of said comparisons and said fault number (Z) to determine the memory area or memory areas, (a, b, c, d) with fault containing data (A, B, C, D).

The Examiner relies on the following references:

Highleyman et al. (Highleyman)	3,596,254	July 27, 1971
Stevens	3,681,578	Aug. 1, 1972
Dooley et al. (Dooley)	5,220,567	June 15, 1993 (filed Dec. 26, 1991)

Claims 1 and 16 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Stevens and Dooley.

Claim 3 stands rejected under 35 U.S.C. § 103 as being unpatentable over Stevens, Dooley and Highleyman.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[2] and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1, 3 and 16 through 21 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case of obviousness. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found

[2] Appellants filed an appeal brief on February 27, 1996. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on June 18, 1996. We will refer to this reply appeal brief as the reply brief. The Examiner stated in the Examiner's letter dated July 8, 1996 that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

In regard to the rejection of claims 1 and 16 through 21 under 35 U.S.C. § 103 as being unpatentable over Stevens and Dooley, Appellants argue on pages 5 through 8 of the brief that there is no suggestion in the prior art to combine Stevens and Dooley to perform the method steps as set forth in Appellants' claim 1. The Examiner points out on pages 3 and 5 of the answer that Dooley teaches the use of a counter for counting the total number of errors detected by an error detecting means for the purpose of isolating the source of errors. The Examiner argues that this teaching is a suggestion to combine Dooley with Stevens.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner

does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Upon reviewing Stevens and Dooley, we fail to find any suggested desirability of modifying Stevens with Dooley's signature detecting method for isolating source of correctable errors to obtain Appellants' invention as recited in claim 1. We note that Stevens teaches a method of fault location and reconfiguration method in a redundant data processors arrangement. As shown in Figure 2, the output of each of the redundant data processors 1, 2 and 3 are supplied to a majority voting circuit 7. In column 2, lines 24-37, Stevens discloses a simple and straight forward manner of operation in which each of the processors processes the same information and thereby the outputs should be identical. In the event of one processor operating incorrectly, there will still be two identical outputs

and the majority voting circuit will select the output corresponding to these two outputs for transmission to the output terminal 8. In column 2, line 61, through column 4, line 7, Steven discloses an isolating circuit 20 that detects a processor which is producing erroneous outputs at a rate above a first predetermined level and then produces an alarm signal or isolates the processor from the processing arrangement. Therefore, Stevens provides a simple method of isolating the source of errors.

On the other hand, Dooley teaches a highly complex signature detecting system for isolating source of correctable errors in a computer system. In column 1, lines 57-62, Dooley teaches that their invention is concerned with maintenance of a computer system constructed of a large number of field replaceable units. Examples of these field replaceable units are edge-connected circuit boards, quick-disconnect cables, rack-mounted replacement boxes and other easily-replaceable components. Dooley teaches in column 5, lines 15-20, that the system provides a signature collection and analysis method which helps field engineers to make more intelligent decisions regarding which field replaceable units is most likely to be responsible for causing an unusual high number of self-correctable errors. We note that Dooley is

not concerned with using redundant processors where each processor processes the same information, but instead Dooley is concerned with maintenance of a computer system having field replaceable units.

We do not agree that those skilled in the art would have been led to use the highly complex signature detecting method to isolate the source of error as taught by Dooley in the simple Stevens fault location system using redundant processors. The Examiner reasons that Dooley's teaching of fault isolation is by itself a suggestion for combinability. However, this does not answer the question of desirability of such a modification when Stevens provides for a more simple method of fault isolation. We fail to find a suggestion in the prior art to combine Stevens with Dooley, and thereby we will not sustain the Examiner's rejection.

In regard to the rejection of claim 3, we note that the Examiner has relied upon the combinability of Stevens and Dooley to obtain Appellants' claimed invention. Since there is no evidence in the record that the prior art suggested the desirability of such a modification, we will not sustain the Examiner's rejection of claim 3 as well.

We have not sustained the rejection of claims 1, 3 and 16 through 21 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
RICHARD TORCZON Administrative Patent Judge	)	

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